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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,515	12/05/2003	Nobuo Nakamura	245592US-2SRD DIV	7844

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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,515	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *11-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/30/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-10 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 6,690,423 (Nakamura et al.) in view of Applicant's Admitted Prior Art (AAPA) (figs.1 and 2A).

In regards to claim 1, Nakamura et al. disclose a semiconductor device. It comprising: a solid-state image pickup apparatus which incorporates a semiconductor substrate having an image pickup region including unit pixels disposed in a two-dimensional configuration and signal scanning sections for reading signals from the unit pixels in the image pickup region (lines 1-5 of claim 1 of Nakamura et al.), the solid-state image pickup apparatus comprising: a photoelectric conversion region having a first-conduction-type signal accumulating section formed at a position apart from a top surface (the interface between the semiconductor substrate and a substance formed on the active surface of the semiconductor substrate) of the semiconductor substrate in a direction of a depth of the semiconductor substrate for a predetermined distance and

arranged to accumulate signal charges obtained from photoelectric conversion (lines 7-13 of claim 1 of Nakamura et al.); a gate electrode of a first-conduction-type MOS field effect transistor formed adjacent to the photoelectric conversion region and arranged to discharge a signal charge from the first-conduction-type signal accumulating section (lines 14-17 of claim 1 of Nakamura et al.); a first-conduction-type detecting node section serving as a drain region for receiving the signal charges from the photoelectric conversion region via the gate electrode (lines 18-21 of claim 1 of Nakamura et al.); at least a part of the first-conduction-type signal accumulating section in a direction of a channel thereof extends to overlap the gate electrode in a direction in which signals are discharged (lines 22-25 of claim 1 of Nakamura et al.); modulation of the potential of the gate electrode is used to discharge signals from the first-conduction-type signal accumulating section through the channel of the MOS field effect transistor (lines 26-29 of claim 1 of Nakamura et al.); and the first-conduction-type detecting node section is not located below the gate electrode but at a second side of the gate electrode opposite to a first side of the gate electrode formed adjacent to the photoelectric conversion region (lines 30-32 of claim 1 of Nakamura et al.).

Nakamura et al. differ from the claimed invention by not showing a barrier layer formed at least close to a lower part of the first-conduction-type detecting node section of the MOS field effect transistor.

AAPA discloses a barrier layer (a portion of the p-type region [4] formed under the signal detecting section [12]) formed at least close to a lower part of the first-conduction-

type (n-type) detecting node section [12] of the MOS field effect transistor in figs. 1 and 2A.

Since both Nakamura et al. and AAPA teach a MOS transistor with a photoelectric conversion region, it would have been obvious to have the barrier layer of AAPA in Nakamura et al. because it prevents the channel current leaking into the lower portion of the semiconductor substrate.

In regards to claim 2, Nakamura et al. (entire claim 2) further disclose a diffusion-layer region which is formed adjacent to the top surface of the semiconductor substrate above the first-conduction-type signal accumulating section, which has a second-conduction-type opposite to the conduction type of the first-conduction-type signal accumulating section and which contains impurities at a concentration which is higher than the concentration of impurities contained in the channel region of the first-conduction-type MOS field effect transistor.

In regards to claim 3, Nakamura et al. (entire claim 3) further disclose wherein a length of a portion of the first-conduction-type signal accumulating section extending to overlap the gate electrode in the direction in which signals are discharged is shorter than 1/2 of a length of the gate electrode of the first-conduction-type MOS field effect transistor.

In regards to claim 4, Nakamura et al. (entire claim 4) further disclose a length of a portion of the first-conduction-type signal accumulating section extending to overlap the gate electrode in the direction in which signals are discharged is shorter than 1/2 of a length of the gate electrode of the first-conduction-type MOS field effect transistor.

In regards to claim 5, Nakamura et al. (entire claim 5) further disclose a length of a portion of the first-conduction-type signal accumulating section extending to overlap the gate electrode in the direction in which signals are discharged is longer than 1/2 of a depth of a junction of the diffusion-layer region from the top surface of the semiconductor substrate.

In regards to claim 6, Nakamura et al. (entire claim 6) further disclose the first-conduction-type signal accumulating section has a first region formed below the gate electrode and a second region formed at a position except for a position below the gate electrode, and a depth of the first-conduction-type signal accumulating section in the first region from the top surface of the semiconductor substrate is smaller than a depth of the first-conduction-type signal accumulating section in the second region.

In regards to claim 7, Nakamura et al. (entire claim 7) further disclose the first-conduction-type signal accumulating section has a first region formed below the gate electrode and a second region formed at a position except for a position below the gate electrode, and a depth of the first-conduction-type signal accumulating section in the first region from the top surface of the semiconductor substrate is smaller than a depth of the first-conduction-type signal accumulating section in the second region.

In regards to claim 8, Nakamura et al. (entire claim 8) further disclose the first-conduction-type signal accumulating section has a first region formed below the gate electrode and a second region formed at a position except for a position below the gate electrode, and a depth of the first-conduction-type signal accumulating section in the

first region from the top surface of the semiconductor substrate is smaller than a depth of the first-conduction-type signal accumulating section in the second region.

In regards to claim 9, Nakamura et al. (entire claim 9) further disclose the first-conduction-type signal accumulating section has a first region formed below the gate electrode and a second region formed at a position except for a position below the gate electrode, and a depth of the first-conduction-type signal accumulating section in the first region from the top surface of the semiconductor substrate is smaller than a depth of the first-conduction-type signal accumulating section in the second region.

In regards to claim 10, Nakamura et al. (entire claim 10) further disclose the first-conduction-type signal accumulating section has a first region formed below the gate electrode and a second region formed at a position except for a position below the gate electrode, and a depth of the first-conduction-type signal accumulating section in the first region from the top surface of the semiconductor substrate is smaller than a depth of the first-conduction-type signal accumulating section in the second region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
July 9, 2005

Steven Loke
Primary Examiner

LIST OF RELATED CASES

	Docket Number	Serial or Patent Number	Filing or Issue Date	Patent Appl. Publication No.	Inventor/ Applicant
Loke	245592US2SRD DIV*	10/727,515	12/05/03	2004-0108502	NAKAMURA et al.
Loke	268990US2S	11/095,592	04/01/05		YAMAGUCHI et al.

Examiner: Loke Date: 7/9/05

*Present Application; listed for information

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